



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/561,952

06/12/2006

Sho Kumagai

Q92253

3190

23373 7590 11/27/2009  
SUGHRUE MION, PLLC  
2100 PENNSYLVANIA AVENUE, N.W.  
SUITE 800  
WASHINGTON, DC 20037

EXAMINER

LANGMAN, JONATHAN C

ART UNIT

PAPER NUMBER

1794

NOTIFICATION DATE

DELIVERY MODE

11/27/2009

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

sughrue@sughrue.com  
PPROCESSING@SUGHRUE.COM  
USPTO@SUGHRUE.COM

<b>Office Action Summary</b>	<b>Application No.</b> 10/561,952	<b>Applicant(s)</b> KUMAGAI ET AL.	
	<b>Examiner</b> JONATHAN C. LANGMAN	<b>Art Unit</b> 1794	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10 September 2009.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-7 and 9 is/are pending in the application.
- 4a) Of the above claim(s) 4-7 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                        | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 10, 2009 has been entered.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by, or in the alternative, rejected under 35 U.S.C. 103(a) as being unpatentable over Kojima (JP 2000-243706).

Kojima teaches a dummy wafer comprising CVD SiC coated with CVD SiC ([0025]-[0026]). The surface roughness of the outer coating is controlled to have a surface roughness of 1-10 microns (Table 1, and [0024]). This surface roughness allows for compounds such as silicon nitride, which come into contact with the silicon carbide dummy wafer during processing, to adhere strongly. Since the silicon nitride

Art Unit: 1794

can adhere stronger, this allows for subsequent uses without washing steps in between ([0024] and [0033]).

Kojima go on to teach that thicknesses of the SiC film are preferably controlled to be between 20 and 80 micrometers. Example 2 of Kojima is a CVD Sic substrate coated with a 40 micron thick CVD SiC coating that comprises a surface roughness of 4.5 microns ([0025], [0026], and Table 1). A thickness of 40 microns falls within the instantly claimed ranges of between 20 microns or more and 70 microns or less, as claimed in claim 1, as well as, between 20 microns or more and 40 microns or less as claimed in claim 9. A surface roughness of 4.5 microns anticipates the instantly claimed range of 1-10 microns.

Kojima do not teach that the substrate is formed by sintering a mixture containing a silicon carbide powder and a non metallic sintering aid; however these limitations are construed to be product by process limitations. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.”, (In re Thorpe, 227 USPQ 964,966). Once the Examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious

Art Unit: 1794

difference between the claimed product and the prior art product (In re Marosi, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983), MPEP 2113).

As described above, Kojima teaches a CVD sic substrate. CVD SiC is known in the art to be a dense SiC structure free of metals. The resultant material of the instantly claimed sintered mixture of silicon carbide powder and a non metallic auxiliary is also a sintered metal free SiC. Therefore it is the Examiner's position that Saito and the instantly claimed structure are similar, and therefore the final product of Kojima anticipates the instantly claimed final product; wherein the product by process steps are said to not provide a patentable distinction between the instantly claimed dummy wafer and that of the prior art.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotate et al. (US 5,448,418) in view of Coppola (US 4,124,667) or Otsuki et al. (6,090,733).

Hotate et al. teach a structure as seen in Figure 1, which comprises a bulk material, 1, completely coated on all sides with a layer, 2, which comprises a top

Art Unit: 1794

surface 3. The bulk material comprises SiC in the shape of a rectangular plate having a size of 100mmx300mmx20mm 9col. 2, lines 35-40). The teaching of Hotate that the SiC body is shaped (col. 3, lines 1-10), implies that the body is cast into a desired shape and then sintered to form a desired shape as is known in the art. Hotate teach that the bulk material is coated with a CVD SiC coating with a surface roughness of 0.1 nms (col. 3, lines 20-25). The coating of sample 2 is a single coating (col. 3, lines 25-30) and as seen in Table 1 (col. 4, lines 58), the coating of sample 2 has a thickness of 30 microns which falls within the applicants instantly claimed range.

Hotate fails to teach that the coated substrate is a “dummy wafer”. However, the mirror of Hotate has all of the same structure as instantly claimed, and the applicant has not defined the term “dummy wafer”. The term “dummy wafer” is merely a descriptive term that does not imply any structural limitations to the claimed article, and therefore the mirror of Hotate is said to read on the claims as presented.

Hotate fails to teach that the bulk material comprising SiC is formed by sintering a mixture containing a silicon carbide powder and a non metallic sintering auxiliary.

Coppola et al. teach that sintered shaped bodies of silicon carbide can be formed by shaping bodies of silicon carbide powder and phenolic resin (abstract). Phenolic resin is taught by the applicant to be a non metallic sintering auxiliary (instant specification, page 3, lines 14 and 15).

It would have been obvious to a routineer in the art to provide the shaped SiC body of Hotate et al. by any known means in the art, including that which is taught by

Art Unit: 1794

Coppola, as Coppola has shown that these are known and obvious methods of forming SiC bodies in the art.

Alternatively, Otsuki et al. teach that using non metallic sintering aids are known in the art of forming sintered SiC compacts (See at least the abstract of Otsuki et al. (6,090,733)). Otsuki teaches that by using nonmetallic sintering aids in SiC as opposed to using metallic sintering aids, the resultant SiC will have less contamination (col. 3, lines 12-18). Accordingly, it would have been obvious to one having ordinary skill in the art to employ non-metallic sintering aids in the SiC compact of Hotate, since Otsuki teaches that such sintering aids are conventionally used in the art and, moreover, that non-metallic sintering result in compacts having desirable properties, e.g., less contamination (Otsuki, col. 3, lines 12-18).

Claims 1, 2, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotate et al. and Coppola or Otsuki, as applied above, in view of Wakugawa (US 4,856,887).

As described above, Hotate teaches forming rectangular plates of SiC coated with CVD SiC. Hotate, does not describe the mirror to be a "dummy wafer", however, as described above, no structural limitations are given to the term "dummy wafer". Even if structural limitations were to be construed from the descriptive term "dummy wafer", which the Examiner does not contend to be true, it is known in the art to form mirrors in the same shapes which are described within the instant specification.

Wakugawa et al. teach lightweight mirrors comprising Sic cores, coated with CVD SiC as an outer layer (abstract). As seen in figure 1, the mirror of Wakugawa has the same shape as instantly described (col. 2, lines 29-30).

It would have been obvious to a person having ordinary skill in the art at the time the present invention was made to form the mirrors of Hotate in to circular shapes, as Wakugawa has shown that circular mirror are commonly used in the art, and this would have been an obvious design choice for a routineer in the art.

Claims 1, 2, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 5,853,840) in view of Kojima (JP 2000-243706).

In regards to claims 1 and 9, Saito et al. teach a dummy wafer comprising a sintered SiC material (1), which is coated on at least one surface with a silicon carbide layer (2) formed by CVD (abstract and col. 3, lines 19-30). Saito et al. teach that the dummy wafer (1) is formed of non-metallic materials such as phenolic resins (col. 2, lines 15-22), and therefore results in dummy wafers that contain no metal to become a contamination source for semiconductor wafers (abstract).

Although Saito et al. do not teach forming the bulk(1) by sintering silicon carbide powder and a non metallic sintering auxiliary as instantly claimed, these limitations are construed to be product by process limitations. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious

Art Unit: 1794

from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.”, (In re Thorpe, 227 USPQ 964,966). Once the Examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product (In re Marosi, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983), MPEP 2113).

As described above, Saito teaches a sintered metal free SiC. The resultant material of the instantly claimed sintered mixture of silicon carbide powder and a non metallic auxiliary is also a sintered metal free SiC. Therefore it is the Examiner's position that Saito and the instantly claimed structure are one in the same.

Saito et al. teach that the dummy wafer can be subjected to a surface treatment in order to improve the surface condition, including lapping, polishing etc. (col. 3, lines 37-43). However, Saito fails to teach a specific surface roughness, specifically one of 10 microns or less.

Kojima teaches a dummy wafer in the same are as Saito. Kojima teaches a dummy wafer comprising CVD SiC coated with CVD SiC ([0025]-[0026]). The surface roughness of the outer coating is controlled to have a surface roughness of 1-10 microns (Table 1, and [0024]). This surface roughness allows for compounds such as silicon nitride, which come into contact with the silicon carbide dummy wafer during processing, to adhere strongly. Since the silicon nitride can adhere stronger, this allows for subsequent uses without washing steps in between ([0024] and [0033]).

Art Unit: 1794

It would have been obvious to a person having ordinary skill in the art at the time the present invention was made to control deposition and or post processing of the CVD film of Saito in order to obtain a coating with a surface roughness of 1-10 microns as this surface roughness has been shown to provide longer uses for the dummy wafer, between washes, and therefore would reduce production costs.

Saito fail to teach a thickness of their CVD SiC layer.

Kojima go on to teach that thicknesses of the SiC film are preferably controlled to be between 20 and 80 micrometers and teach specific examples with a thickness of 40 microns in Example 2. Kojima teach that these thickness ranges help to control the average surface roughness and the thickness of the SiC can be made uniform ([0020]).

It would have been obvious to a person having ordinary skill in the art at the time the present invention was made to deposit the CVD SiC layer of Saito to a thickness of 20-80 microns, or more specifically 40 microns, as this thickness has been shown to aid in obtaining desired surface roughnesses, as explained above, as well as providing uniform coatings.

In regards to claim 2, Saito teaches that by forming the CVD SiC layer on the SiC wafer, a dummy wafer with higher purity is obtained. Saito et al. are silent to forming the CVD layer on the entire substrate including side surfaces.

It would have been obvious to a person having ordinary skill in the art at the time the present invention was made to coat the entire substrate of Saito, as this would result in the highest purity dummy wafer.

Art Unit: 1794

Furthermore, as is known in the art, and been established by the examiner in the previous office actions, sintered SiC has open pores and coating the entire surface area would seal the pores. During semiconductor processing steps, these pores would offer sites for contamination and lower the production lives of dummy/monitor wafers. Sintered SiC also has high contents of impurities as is known in the art; much higher concentrations than CVD SiC. By coating the entire sintered substrate with CVD SiC, one would obtain increased resistance to known chemicals and atmospheres of semiconductor manufacturing apparatuses. Such endeavor would likely increase productivity by producing higher numbers of non contaminated wafers when CVD SiC coated dummy wafers are used alongside production wafers in manufacturing.

### ***Response to Arguments***

The applicant's arguments were found persuasive in regards to the rejections involving Lu. Lu teaches forming thick CVD SiC coatings of 1 mm or more for larger production pieces. Therefore it would not have been obvious to modify the thickness of Lu to include those ranges instantly claimed.

Applicant's arguments with respect to claims 1, 2, and 9 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN C. LANGMAN whose telephone number is

Art Unit: 1794

(571)272-4811. The examiner can normally be reached on Mon-Thurs 8:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer McNeil can be reached on 571-272-1540. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JCL

/Timothy M. Speer/  
Primary Examiner, Art Unit 1794